#22/Dec. 9/25/02

IR-1609 (2-1941)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of
Daniel M. Kinzer
Serial No.: 09/292,186 Group Art Unit: 2811
Filed: April 15, 1999 Examiner: S. Hu
For: P-CHANNEL TRENCH MOSFET STRUCTURE

-

Assistant Commissioner for Patents
Washington, D.C. 20231

DECLARATION OF RITU SODHI UNDER 37 C.F.R. §1.132

Sir:

I, Ritu Sodhi, residing at 2219A Harriman Lane, Redondo Beach, declare that:

1. I am a Design Manager employed by International Rectifier Corporation, 233 Kansas Street, El Segundo, California 90245, the assignee of the subject patent application. My duties include leading the MOSFET design group responsible for developing power MOSFETs for DC-DC converter applications for, among others, computers, network communications, and power load management applications. As part of my duties, I propose and develop new device technologies, supervise a team of senior design and process engineers, lead, and participate in, the technology development discussions, oversee the development and release of new technology platforms, and facilitate the transfer of these technologies to production.

2. I have a PhD degree in Electrical Engineering from Rensselaer Polytechnic Institute. In the course of my employment with International Rectifier Corporation, I have worked in the design and production of semiconductor devices, and in particular vertical channel MOSFETs. I am familiar with the technical details surrounding the formation of N-channel and P-channel vertical MOSFET devices, including the device that is the subject of the present invention.

3. I understand that the Patent Examiner assigned to examine the above-identified patent application has rejected claims 1, 3-6, 8-13 and 20-22 as being obvious over the disclosure by Floyd et al. (U.S. Patent No. 6,090,716). I further understand that the Patent

Examiner considers the structure of the present invention to be an obvious variation of the structure disclosed by Floyd et al. with the polarity of the device reversed.

4. I have reviewed U.S. Patent No. 6,090,716 to Floyd et al., entitled Method of Fabricating a Field Effect Transistor.

5. Floyd et al. teach an N-channel vertical trench-type MOSFET device.

6. The differences between the MOSFET device disclosed by Floyd et al. and the one presented in this patent are significant. A number of additional steps and further design effort would have to be undertaken to obtain a workable P-channel device following a polarity conversion of the N-channel MOSFET device disclosed by Floyd et al. As an example of some of the differences provided in the construction of the P-channel device according to the present invention, the following facts are offered.

a) Floyd et al. have used an SOG plug to isolate the polysilicon gate from the source metal, while our process uses a photolithography-defined contact to the source and base region.

b) The structure disclosed by Floyd et al. Does not show a contact to the base of the MOSFET, which would make the MOSFET extremely prone to avalanche failure. In our proposal, the contact to the base region is made using a silicon etch step, which is much more difficult to accomplish with the 1um deep source junction used by Floyd et al.

c) The structure of the present invention has the source implanted after trench formation, simultaneously doping the poly. By arranging operations in this way, the source is maintained shallow (0.35um vs. 0.97um), which reduces the input capacitance.

d) There is no mention of the termination structure in the disclosure by Floyd et al. The present invention has a trench termination structure for the P-channel technology, the termination trench and active gate trench being etched simultaneously.

e) The claimed structure uses boron doping for the polysilicon in the gate, to maintain low threshold voltage (Vth). Floyd's proposal shows the use of phosphorus implant, followed by the use of boron nitride (as a source of boron), which indicates that the boron will likely saturate the gate oxide, leading to Vth instability.

7. In addition, fabrication of a P-channel vertical trench-type MOSFET device is more challenging than the construction of an N-channel vertical trench-type MOSFET device. For example, in N-channel devices, the substrate is an Arsenic-doped material. In P-channel devices, the substrate is Boron-doped material. During the various thermal steps

needed to fabricate the MOSFET, Boron from P-channel substrates out-diffuses into the N-type epi region much more readily than Arsenic from N-channel substrates. Since the MOSFET channel is defined by this epi, any variation in the out-diffusion directly impacts the blocking capability and the threshold voltage of the device. In addition, the doping in the polysilicon needs to be carefully optimized to better control the threshold voltage of the P-channel device. Hence, there is more control and characterization needed for P-channel MOSFETs, in particular if a rugged and stable device is to be produced.

8. Accordingly, notwithstanding the contention by the Patent Examiner that a MOSFET design that works under one polarity type is also normally workable under the reverse polarity, a number of additional steps and experimentation must be undertaken to construct a P-channel vertical trench-type MOSFET in accordance with the disclosure of the present invention. The additional steps and experimentation required represent a significant design challenge and require far more sophistication than merely reversing the polarity of an N-channel device.

9. The technology described in the subject application has been used in the production of products that have been sold by, and continue to be sold by International Rectifier Corporation. The technology of the present invention is incorporated into four different products sold by International Rectifier Corporation, each of which has been highly commercially successful. The following Table summarizes the product, the number of units sold, and the total revenue generated for each product.

IR NUMBER	TOTAL VOLUME	TOTAL REVENUE
IRF7210	81.2K	$68K
IRF7220	60.6K	$37.3K
IRLMS4502	430K	$64.8K
IRF7233	32M	$5.834M

10. As evidenced by the above data, sales of products incorporating the technology of the subject invention total in excess of $6,000,000. These results provide clear evidence of commercial success for the technology of the subject application.

11. Accordingly, I conclude that the present invention is not an obvious variation of the disclosure provided by Floyd et al., but rather requires further steps and

experimentation to achieve the specified result, and has produced widespread commercial success.

12. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-referenced application or any patent issuing thereon.

Dated: 9/4/02

Ritu Sodhi

Ritu Sodhi